Advanced packaging yields higher performance and reliability in power electronics

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A B S T R A C T

Power density of power electronics will continue to grow. It is always supported by progress in power semiconductors. Further significant loss reduction of IGBT and diodes becomes possible if power circuit design improves with respect to electro-dynamic performance. Efforts to improve cooling for better power dissipation out of smaller volumes appear to be disadvantageous in comparison to increase of junction temperature. The direction of increasing junction temperature is most effective for air cooled systems as well as liquid cooled systems with high ambient temperature. To enable long life time of modules under higher operation temperature heavy copper wire bonding and diffusion soldering of chips are presented to fulfill the requirements. New chip technologies with integrated heat buffers ensure transient thermal capability for shrunk power chips.

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1. Introduction

Growth of power density is a major trend in power electronics [1]. In inverters and converters for variable speed drives, regenerative energies and other application, evolution of IGBT and accompanied freewheeling diodes in module packages determine the progress. Increasing power density means increasing current density for these devices. Fig. 1 exemplarily demonstrates the progress in current density of IGBT-modules from 1993 until today. Trench and field-stop IGBTs – actual IGBT4 – represents the state of the art [3]. With 1200 V-IGBT4 higher junction temperature for operation (\(T_{J,op}\)) of 150 °C became possible. It generated a remarkable step to higher current.

Potential for further progress in IGBT and diode technologies exists. Three main levers can be identified: loss reduction by minimizing wafer thickness and optimizing cell design [2], improving thermal impedance and third increasing maximum junction temperature to allow for higher difference in temperature from junction to ambient. All three paths for improvement depend strongly on design of power circuits, assembly and interconnect technologies of modules [1,3]. A consequence rising current density and shrinking chip thicknesses is a decreasing thermal capacitance of the power semiconductors. Thermal capacitance of the semiconductor chip is beneficial for high power transients in the time frame of up to a few milliseconds. For short circuit conditions, where full bus voltage and 4–6 times rated current are present at the chip simultaneously for up to 10 μs the thermal capacitance of the chip has to absorb the energy in today's modules. Today, heat transfer out of the chip into the interconnect layers on a time scale of some 10–100 μs after the initial stress is limited, requiring high thermal capacities of the silicon itself [13]. Again assembly and interconnect technologies are challenged to contribute to the progress in semiconductor devices.

2. Power circuit design for loss reduction

The vertical concept of IGBT [2] and diode becomes optimum, when a rectangular distribution of electrical field is met in blocking state. It results in the minimum wafer thickness required for a certain blocking voltage. In conjunction with cell optimization, it leads to a minimum \(V_{CEsat}\) as well as low switching losses. Following this path would lead to snap-off of current during switching, as long as stray inductance in power circuit does not become reduced, significantly. Therefore, further loss reduction of power devices requires better design of power circuits with respect to electrodynamics [3]. Module and power circuit strictly have to follow strip line principles (Fig. 2). This will also have the benefit of best current sharing among paralleled devices and will result in less EMI. An inverter concept following these principles has been presented in [4]. The concept is shown in Fig. 3. It is a half-bridge, whose power terminals are made by rows of press-fit pins [8,9] to allow for contact along a line-interface between inner and outer strip line. The switching behavior improved significantly (Fig. 4) in comparison to switching in standard power circuit design (Fig. 5). The strict strip-line design of power circuits not only enables further improvement of Si-devices but is also a prerequisite for the application of fast switching wide band-gap devices based on SiC, GaN, etc.

3. Lower thermal resistance for higher power dissipation

Starting from air cooled systems thermal resistance can significantly improve by going to liquid cooling of the heat sink. Even
best air cooled heat sinks cause almost twice as much thermal resistance as internal to the module, which is assembled on it. Liquid cooled heat sinks with an adequate internal structure, that spreads heat and offers an extended cooling area for the liquid, can lower the heat sink’s contribution to about a third of the air cooled version. When dealing with liquid cooling eliminating thermal grease at the interface module to heat sink becomes the next attractive step for improvement. It requires the heat sink to be directly joined to the module, i.e. replacing the base plate of the module by a heat sink [1,16]. It leads to another improvement up to a factor of two. Either a base plate with pin fin structure (Fig. 6) or a closed heat sink with an inner pin fin structure (Fig. 7) can result in such improvements. It has to be understood, that a very good thermal resistance at an attractive low pressure drop requires always a pin fin structure that spreads heat, before entering the cooling liquid. Systems with liquid cooling and integrated heat sinks can reach such low thermal impedance that even for alumina as insulator inside the module the thermal resistance becomes such low, that maximum junction temperatures cannot be reached when operating within the SOA of the power semiconductors and at typical switching frequencies.
Thermal resistance can become even lower by AlN or Si₃N₄ as internal insulator. Both nitride-materials are used in modules today. These materials do not make much sense in air cooled systems as the improvement in total thermal resistance would be low and would not justify the cost increase related to these materials. For liquid cooled systems the improvement may still not justify the cost increase.

Cooling power semiconductors from both sides is a well known method for hockey puck packages. Nowadays 2-side cooling is reconsidered for automotive applications. It can be questioned if the high mechanical precision and complex circuit design involved with this cooling concept is acceptable. It might hinder the optimization of the power circuit design towards lowest inductance and perfect current sharing among paralleled devices. The two-side cooling principle is also in conflict with well established production methods for power modules. A module design that clearly separates electric and thermal paths is the better way to meet all design and manufacturing requirements and it can achieve low enough thermal resistance.

4. Higher $T_J$ for higher power dissipation

The most effective way to increase power density in air cooled systems (Fig. 9) is to operate at higher $T_J$ [1]. The heat that can be dissipated varies with the difference in temperature from junction to ambient and will simply grow with $T_J$ (Fig. 8). Increasing $T_J$ is also very attractive in liquid cooled systems, where the ambient temperature, i.e. the temperature of the cooling liquid is at an elevated level. An example is the hybrid vehicle application, where the coolant becomes heated by the combustion engine. This effect becomes especially pronounced, when combustion engine and power electronics use the same cooling circuit [1].

The path towards higher junction temperatures is feasible from the device point of view, as well as for Si-devices as for SiC, GaN-devices [5–7]. Assembly and interconnect technologies, i.e. Al-wire bonding and soft soldering are limiting the range of temperature and swing in temperature [1]. Under varying load, which is tested by power cycling, three major failure mechanisms take place (Figs. 10a–c). First, it is the well known wire bond lift-off, which is caused by the weakness of pure Aluminum and the miss-match in thermal expansion between Si and Al. Second it is the solder degradation under the chip, which is caused by the weakness of soft solder and the miss-match in thermal expansion between solder, Si and substrate. Third it is the degradation of solder between Cu-base-plate and substrate, which is caused by the weakness of soft solder again and the difference in thermal expansion between base plate and substrate [1,10,14].

5. Higher $T_J$ and reliability by new packaging technologies

For an utilization of devices at higher junction temperatures, which is not limited by wear out during power cycling a new wire bonding technology, a new die attach method and a new substrate to base plate attach method has been developed and presented in [10–12]. In conjunction with new chip technologies and chip metallization, as described in [13], further increase of current density in chips becomes possible. The new assembly and interconnect technologies are heavy copper wire bonding on IGBT and diode...
chips, diffusion soldering as die attach method and an improved substrate soldering method.

The copper wire bond technology eliminates the lift-off problem because of the higher mechanical strength of copper and less miss-match in thermal expansion. Diffusion soldering turns soft solder into Sn–Cu–X-alloys during the process, again resulting in much higher mechanical strength. It eliminates the solder degradation under the chip.

The new substrate solder joint is strengthened by an inner anchor structure. The failure mechanism for the substrate to base plate joint continues to exist in principle but the lifetime of modules with base plate is extended significantly to meet the targets as deducted from the extended temperature range. Fig. 11 illustrates a module (PrimePACK™2), which contains the three new module technologies as well as the new chip technologies. The power terminals are also Cu–Cu-bonded [15], which supports the larger power cycling capability, as well.

The reliability of the new technologies is proven by several power cycling tests (Fig. 12), where some of them are completed and others are still running. One group of tests dealt with modules without a base plate to study the copper wire bonds in combination with the diffusion solder layer under the chip excluding any influence by the substrate to base plate joint. These tests reached around 1 million cycles to failure, which represents a new benchmark and gives comfortable room for $T_J$-increases. A new failure mechanism occurred. The copper metallization of the substrate is delaminating from the back side of the substrate. The wire bonds and die joints remained unchanged [10–12].

Another group of tests dealt with modules with copper base plates. These tests, were done with longer cycle times in the minute range to stress the substrate to base plate joint by power cycling. Such modules reach 100,000 cycles at a $T_J$ of 130 K, which means an improvement, which enables the increase of junction temperatures. In a first step the new technologies are intended to provide a new power cycling capability that is 10 times higher than today, which will be characteristic for the first products coming along. These Infineon products can be identified by the extension .XT.

6. New chip technologies enabling new packaging technologies

New front side and back side metallization are required. To allow wire bonding of thick Cu wires the standard Al metallization is too soft to reliably bond Cu wires. Therefore a Cu surface had to be established on the front side of Chips. For the back side again an adequate metallization was required to support the alloying of soft
solder during die attach. The new front side metal serves also as additional heat capacitance for the chip. As this additional heat capacitance is directly attached to the chip surface and each active cell transfer of heat out of the active region volume of the chip is very fast. It can buffer heat from high and short transient loads like under short circuit. The new die attach to the substrate in addition gives a lower thermal impedance between chip and substrate, where a thick layer of copper exists[13]. The lower thermal impedance is a consequence of the much thinner diffusion soldered layer. Instead of relying on heat capacitance of Si, heat capacitance external to the active semiconductor is installed. This external heat capacitance is in very good thermal contact to the active semiconductor. Thus shrink of active semiconductor volume is possible and current density can grow.

7. Conclusion

Power density and related current density can continue to grow. New module and power circuit design can support faster switching of Si and wide band-gap devices leading to lower losses and chip shrink.

Thicker chip metallization and lower thermal impedance between chip and substrate will compensate for lost heat capacitance within the active semiconductor.

Heavy copper wire bonding and diffusion soldering eliminate today’s failure mechanisms in power cycling. Both together can be regarded a breakthrough in assembly and interconnect.

Improved substrate to base plate soldering together with the new Chip assembly and interconnect enable the increase of junction temperature or longer lifetime in severe applications.

From the thermal considerations increase of junction temperature is the most cost effective and attractive way to support higher power and current density.

References