A green-switch controller IC for cascade buck–boost converter with seamless transition over entire input and load range

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ARTICLE INFO

Article history:
Received 24 December 2010
Received in revised form 2 June 2011
Accepted 14 June 2011
Available online 18 July 2011

Keywords:
DC power systems
Integrated circuit design
Power electronics
Switched mode power supplies

ABSTRACT

To raise the utilization ratio of lithium-ion battery in portable devices, a novel green-switch controller IC is proposed to constitute a 4-switch cascade buck–boost prototype, which is capable of outputting non-inverting step down and step up voltages. According to the relations between the input and output voltages through duty ratio, a finite state machine automatically determines the work method of converter namely buck method, boost method or transition method by combining peak and valley current programmed mode so as to improve the line regulation over the entire input voltage range. A three-phase seamless transition method is introduced into the controller. Its additional advantage is to lower output ripples. Furthermore, a special burst mode is added to reduce the power consumption during light-load operation. An elaborately designed circuitry and rigorous stability analysis further improves the seamless performance. The controller IC is designed and fabricated in 1.5 µm BCD (Bipolar-CMOS-DMOS) technology with an area of 8.75 mm² and applied to a 2.7 V–4.2 V/3.3 V, maximum output power 1.65 W buck–boost converter. It features over 90% conversion efficiency during normal application and still remains over 80% under standby mode. The experimental results show that all functional and performance targets are successfully achieved as expected.

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1. Introduction

Raising the efficiency of utilization of battery is of most importance to modern portable devices powered by lithium-ion batteries, such as Personal Digital Assistants (PDAs), cellular phones and media players [7,15]. Since the efficiency of utilization strongly depends upon the performances of the power management (PM) system of the devices, it brings more challenges to power management designers.

As is well known, the DC–DC converter is usually indispensable in a Li-ion battery PM system for that the voltage of Li-ion batteries is 4.2 V while fully charged, and it will reduce to 2.7 V while exhausted. On the other hand, the rated supply voltage of most chips in portable apparatus is 3.3 V. Thus, the converter is required to supply step down and step up power supply voltages so that they can work normally over the entire voltage range of Li-ion batteries [1–19].

Meanwhile, the conventional buck–boost converter usually provides negative output voltage only, which is inconvenient for real power supplies. Several topologies for step down/step up converters were developed. Among them, the Ćuk converter needs two inductors, which is huge in volume and brings about the electro-magnetic interference (EMI). Besides, it also provides inverting voltage only. The SEPIC converter could offer positive output voltage. However it is even huger since it needs two inductor–capacitor filters [2,8–10,27].

In this paper, a 4-switch cascade buck–boost structure is proposed [17–19]. Different from the ones mentioned before, it outputs non-inverting voltage and needs one inductor–capacitor filter only. Based on it, a green-switch buck–boost controller chip is constructed. Controlled by this chip, the converter can transfer from buck method to boost method automatically according to the difference between input and output voltages and vice versa. Furthermore, a three-phase transition method is adopted when input voltage is close to output voltage. This method produces lower output ripple voltage than normal ones, such as traditional buck–boost method or buck/boost interchanging method [3,12–14,16]. Moreover, it features fast response and seamless transition. The multi-mode transition is controlled by a finite state machine. The control strategy implements multi-use of circuitry and simplifies it greatly.

In portable applications, due to the use of high switching frequency, the switching loss constitutes the major part of consumed power in light load condition. Unfortunately, the standby mode or very light load mode is most common for portable apparatus. Thus high efficiency at light load is crucial to prolong the battery lifetime. A lot of efforts have been put into...
its improvement recently [20–26]. A good solution is reducing the switch frequency at light load so as to maintain the converter efficiency close to that at heavy load. Therefore, the pulse width modulation (PWM)/burst multi-mode modulation is adopted in this controller. To improve efficiency and reduce the light-load and standby power dissipation, a two-mode operation, forced continuous current mode (CCM) and high efficiency burst mode, is introduced, which can be user selected to fit specific applications. At heavy load, it works in PWM mode with a constant switch frequency. When the load decreases to a setting level, it transfers into burst mode automatically and maintains the same switch frequency. That is green-switch control method.

The proposed controller integrated circuit (IC) was designed and fabricated in 1.5-μm BCD process with an area of 8.75 mm². It is successfully applied to a 4.2 V/2.7 V input buck–boost converter. Experimental results demonstrate that the steady 3.3 V output with a max error of ±0.06% as well as excellent line regulation is achieved. Also a high efficiency of over 80% is realized from full load down to no-load, with the maximum reaching 94%.

2. Proposed multi-mode operation

The proposed controller adopts single-inductor 4-switch cascade buck–boost architecture to make converter work normally whenever \( V_{IN} \) is above, below or equal to \( V_{OUT} \). The design aim is focused on the controlling of the four switches and the transition between step down and up functions. Thus the constant-frequency fast-response current programmed control mode is used. All operation modes are implemented in single current control loop and voltage control loop. The function diagram of the green-switch buck–boost converter is shown in Fig. 1. The feedback dividing resistors \( R_f_1 \) and \( R_f_2 \), together with error amplifier (EA), build up the voltage loop; its output adding with a slope compensation module (SLOPE) is connected to the current comparator (ICOMP), which is the main component of the current loop. Burst comparator (BURST) composes a hysteresis control loop, which is parallel with the voltage loop to implement high efficiency burst mode operation. The key waveforms in different modes are in Fig. 2. The operation principles in each mode are described in the following subsections.

2.1. 4-Switch cascade buck–boost architecture

The cascade buck–boost converter is shown as the power stage in the Fig. 1. Two possible control methods could be adopted for

![Fig. 1. The proposed system diagram.](image-url)

![Fig. 2. Key waveforms of multi-mode operation: (a) buck mode, (b) boost mode, (c) three-phase transition mode started by buck discharge, (d) three-phase transition mode started by boost charge.](image-url)
this architecture [4–6,11]. One is like a conventional buck–boost converter. It has two operation periods. In period 1, TG2 and BG1 are switched on for charging. In period 2, BG2 and TG1 are switched on for discharging. Since four switches are operating in this mode, the switch loss is heavy.

The second one can be regarded as a buck converter cascading with a boost converter. When \( V_{\text{IN}} \) is above \( V_{\text{OUT}} \), TG1 is always on and BG1 is always off. TG2 and BG2 are switching to implement buck converter. While \( V_{\text{IN}} \) is below \( V_{\text{OUT}} \), TG2 is on and BG2 is off all the time. TG1 and BG1 are switching to implement boost converter. In this mode only two switches are switching every cycle, which results in less switch loss and higher efficiency. Therefore this control mode is adopted in this paper.

In addition, while \( V_{\text{IN}} \) is close to \( V_{\text{OUT}} \), a three-phase transition method is introduced. In current programmed mode, a seamless transition between the buck and boost method could be achieved by limiting the duty cycle of two modes. The reason to introduce the three-phase transition method is that it not only makes seamless transition over the entire input voltage range but also produces lower output ripple voltage [2].

2.2. Buck and Boost method operation

If \( V_{\text{IN}} \) is much larger than \( V_{\text{OUT}} \), the converter works in buck method. Here the current sense resistor is used to monitor the buck synchronous switch. So the valley current programmed control mode can be adopted. Fig. 2(a) shows the buck current loop control principle.

At every clock edge, BG2 turns on first, the inductor current decreases till it reaches the control value. Then BG2 turns off and TG2 turns on to increase the inductor current. \( V_{\text{SENSE}} \) represents the sensed synchronous switch current through the sense resistor, and it is always negative. Therefore \( V_{\text{CONTROL}} \) should also be negative.

When \( V_{\text{IN}} \) is much smaller than \( V_{\text{OUT}} \), the converter will work in boost method. In boost method, the boost power switch current is sensed by the sense resistor. At every clock edge, BG1 turns on first. The inductor current increases until it reaches the control value. Then BG1 turns off and TG1 turns on to decrease the inductor current. It is called peak current programmed control mode. The loop control principle is shown in Fig. 2(b). Here \( V_{\text{SENSE}} \) is always positive, so is \( V_{\text{CONTROL}} \).

In traditional current mode controller, the \( V_{\text{CONTROL}} \) signal is controlled by voltage loop output, typically the output of error amplifier (EA_OUTPUT). In order to avoid the difficult problem caused by generating negative and positive \( V_{\text{CONTROL}} \). Here \( V_{\text{SENSE}} \) is controlled by EA_OUTPUT, thus simplifies the structure for both buck and boost control. The \( V_{\text{CONTROL}} \) is usually set to a constant, e.g., the ground voltage.

In buck method, the EA_OUTPUT controls a voltage plus on the \( V_{\text{SENSE}} \) and in boost method, controls a voltage minus from \( V_{\text{SENSE}} \). Demand by the negative feedback control, the plus voltage is determined by Eq. (1) and the minus voltage is determined by Eq. (2). \( I_i \) and \( \Delta I \) is inductor current and current ripple, respectively. \( A \) is the voltage gain factor, which can be calibrated to any value according to the control demand:

\[
AV_{\text{EA,OUT}} = \left(I_i - \frac{1}{2} \Delta I\right)R_{\text{SENSE}}
\]

\[
AV_{\text{EA,OUT}} = \left(I_i + \frac{1}{2} \Delta I\right)R_{\text{SENSE}}
\]

It is implied that the inductor current is directly proportional to EA_OUTPUT for both buck and boost method. Based on the similar current sense principles of both two modes, the control circuit can be constructed just by one error amplifier and one current comparator in a single control loop. This could realize the circuit multi-utilization.

2.3. Three-phase transition method operation

When \( V_{\text{IN}} \) is close to \( V_{\text{OUT}} \), a three-phase operation mode is introduced into controller to realize seamless transition and lower output ripple. In three-phase transition method, two additional analog TIMER blocks, T0 and T00, are added to judge the duty cycle.

When the converter works at valley current programmed controlled buck method, the \( V_{\text{IN}} \) vs. \( V_{\text{OUT}} \) relation is expressed as

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} = 1 - D
\]

Here \( D \) is the duty cycle of BG2. In this paper, \( D \) always means the duty cycle of the first switch on time at every clock rising edge. When \( V_{\text{IN}} \) decreases and approaches \( V_{\text{OUT}} \), \( D \) decreases. If \( D \) is less than a fixed value \( D_0 (D_0 = T_0/T) \), here \( T \) is the switch period, switch frequency is 400 kHz and \( D_0 \) is set to about 16% in the design), the converter gets into transition method. In transition method, BG2 and TG1 are firstly turned on as the buck discharge phase. Then a boost charge phase is inserted. It is the second phase, during which BG1 and TG2 are turned on. At last TG1 and TG2 are turned on to form third phase.

The working theory is shown in Fig. 2(c). As the waveform shows, the clock edge triggers the buck discharge phase, and then the inductor current decreases. Note that in this phase the buck control loop is applied. While the control signal level has been reached, the current comparator triggers the boost charge phase and the inductor current starts to increase. This process will end in a constant time \( T_0 \) and then be followed by the last phase, buck charge phase for the rest of clock cycle.

According to charge and discharge balance of inductor, the relation of \( V_{\text{IN}} \) vs. \( V_{\text{OUT}} \) in the transition method can be written as

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{1-D}{1-D_0+D}
\]

In Eq. (4), when \( D \) is half of \( D_0 \), \( V_{\text{IN}} \) is equal to \( V_{\text{OUT}} \). If \( V_{\text{IN}} \) decreases further, so does \( D \). Here another constant time \( T_00 \) is set, which is about half \( T_0 \). While \( D \) drops into \( T_00 \), which means \( V_{\text{IN}} \) is already less than \( V_{\text{OUT}} \), the converter will transfer into the boost method.

The boost to buck transition method is similar to that described above. When the converter works at peak current programmed controlled boost method, the \( V_{\text{IN}} \) vs. \( V_{\text{OUT}} \) relation can be written as

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{1}{1-D}
\]

Here \( D \) is the duty cycle of BG1. Just like in buck method, \( D \) decreases with the increase in \( V_{\text{IN}} \). Thus while \( D \) is less than \( D_0 \) the converter works in the three-phase transition method as shown in Fig. 2(d). Firstly, the boost operation loop controls the boost charge phase to increase the inductor current. Then a buck discharge phase is inserted and the inductor current starts to decrease. At last boost discharge phase is triggered by the finish of the constant time \( T_0 \).

In the transition method the \( V_{\text{IN}} \) vs. \( V_{\text{OUT}} \) relation is

\[
\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{1-D_0+D}{1-D}
\]

Similarly, half \( D_0 \) corresponds to the point where \( V_{\text{IN}} \) is equal to \( V_{\text{OUT}} \), and \( D \) further decreases with the further increase in \( V_{\text{IN}} \). \( D \) being less than half \( D_0 \) means that \( V_{\text{IN}} \) is greater than \( V_{\text{OUT}} \). Then the converter will be back to buck method.
In the design of timers, by setting \( T_{00} \) a little less than half \( T_0 \), hysteresis is formed during mode transition and the stability will be improved when \( V_{IN} \) is quite close to \( V_{OUT} \).

From Eq. (3) to (6), it is shown that during the four operation modes described above, the duty cycle \( D \) between mode transitions could be continuously changing between 0% and 100%. In other words, the seamless transition is successfully implemented.

2.4. High efficiency burst mode operation

In order to enhance the converter efficiency at light-load for portable applications, user selectable burst mode operation is introduced, which turns the switches off intermittently based on load demand to reduce the switch loss [20,22,26]. The burst mode could be realized through clamping the minimum value of valley inductor current in buck method and the minimum value of peak inductor current in boost method regardless of the output load. Note that no matter in valley or peak current programmed control mode, the inductor current is proportional to \( E_{A\_OUT} \) according to Eq. (1)–(2). So the minimum valley and peak current clamping both mean minimum \( E_{A\_OUT} \) clamping.

Taking buck method for example, in valley current programmed mode, when current valley is clamped as Fig. 3 shows, \( V_{OUT} \) will increase. Since the voltage loop including error amplifier is unavailable, the voltage loop will be controlled by the \( BURST \) comparator, which is a hysteresis comparator. When \( V_{OUT} \) is over the setting high level, the converter goes into sleep mode. In sleep mode, \( BG_2 \) and \( TG_1 \) are turned off for current freewheeling till the inductor current falls to zero. This discharge loop will bring in the reverse current, which causes power wasting and low efficiency. Thus, the \( REVERSE \) comparator is applied to sense the reverse current to shut down \( BG_2 \) and \( TG_1 \), and then the load is supplied by the output capacitor alone and \( V_{OUT} \) will decrease. When \( V_{OUT} \) is below the setting low level, the converter goes back to normal buck method.

For boost method, due to its peak current programmed operation mode, when the current peak is clamped at a minimum value, \( V_{OUT} \) will increase. Then the voltage control loop and sleep mode control are working in the same way as in buck method.

According to load conditions, each sleep event can last from a few cycles at very light load to short intervals at moderate load. In these sleep intervals, switching loss is reduced and any other unnecessary circuits are turned off to further reduce the quiescent current.

3. System stability analysis

The chief advantage of the current programmed mode is its simple dynamics. The open-loop transfer function contains one less pole than voltage mode, so it is easy to compensate. The weakness is its susceptibility to noise in the current control signals. This noise can prematurely reset the latch thus disrupt the operation of the controller. Addition of an artificial ramp to the controller can improve the noise immunity of the circuit [27]. Thus stability analysis is necessary especially in the proposed multi-mode buck–boost controller. Ensuring the stable and fast response of converter under each operation mode is of most importance.

3.1. Loop compensation

The system modeling of the programmed mode is shown in Fig. 4. The inner loop is a current loop and the external one is a voltage loop [28–30].

\[ G_c(s) \] represents transfer function of the error amplifier. By comparing feedback signal \( V_B \) with reference signal \( V_{REF} \), the error amplifier generates a control voltage. Through the current loop, the control voltage controls the valley or peak value of the inductor current. The inductor current flows into the power stage to generate the output. Besides, the artificial ramp is added through the current loop. \( G_c(s) \) represents the input voltage’s influence on the output. \( Z_{out}(s) \) represents the load current’s influence on the output.

According to the system modeling, the simplified small-signal open-loop transfer function of the controller is

\[
\text{gain}_{loop}(s) = \frac{R_2}{R_1 + R_2} G_c(s) \frac{1}{R_{SENSE}} \frac{v(s)}{i(s)}
\]

in the equation, the first factor is the divided ratio of output to feedback. \( G_c(s) \) is the transfer function of the voltage loop. Then \( 1/R_{SENSE} \) represents the approximate gain of the current loop. At last \( v(s)/i(s) \) describes the loop gain transfer function of the power stage.

Firstly, take the boost topology as an example. According to system modeling with some relative parameters, and through the state-space averaging method [27], the transfer function \( v(s)/i(s) \) of the boost power stage can be found out as

\[
v(s) = \frac{D R}{2} \left( \frac{1}{1 + (1/2)sRC} \frac{1}{1 - \frac{sl}{D^2 R}} \right)
\]

\[
p_0 = \frac{2}{RC} \quad z_0 = \frac{D^2 R}{L}
\]

There is an output pole and a right-half-plane zero in the power stage transfer function, shown as Eq. (9). Here the right half plane zero will significantly reduce the phase margin, which results in system instability. Therefore, an operational transconductance amplifier (OTA) constructed PI compensation structure is introduced for \( E_A \) as shown in Fig. 5. \( A \) and \( r_0 \) represent the DC gain and output resistance of \( E_A \), respectively; \( R_C \) and \( C_C \) compose the RC compensation network. The high gain of \( E_A \) enhances the system loop gain and improves the transient response. The transfer function of the PI compensation is

\[
G_c(s) = \frac{A + sR_C C_C}{1 + s(r_0 + R_C) C_C}
\]
pC = \frac{1}{(f_0 + RC)C}; \quad zC = \frac{1}{RC}C
(11)

Due to the high output resistance of EA, there is a low frequency pole and a left-half-plan zero in the transfer function, shown as Eq. (11). The low frequency pole is the system dominant pole after compensation, and the left half plan zero is used to achieve big enough phase margin and cancel the output pole in certain conditions.

Put Eq. (8) and (10) into Eq. (7), the more detailed transfer function is generated as following:

\[ \text{gain}_{\text{loop}}(s) = \frac{R_2}{R_1 + R_2} \frac{A(1 + sR_C C)}{1 + sRC} \frac{1}{(1 + s/2RC) (1 + s/LR)} \]

(12)

Thus there are two poles and two zeroes in the transfer function. The design aim is to determine the circuit parameters to ensure high enough gain and phase margin of the system.

From Eq. (12), the expression of gain bandwidth product (GBW) can be figured out

\[ \text{GBW} = \frac{1}{2\pi} \frac{R_2}{R_1 + R_2} \frac{AR_C}{1 + sRC} \frac{1}{C} \]

(13)

It shows that no load current parameters in the Eq. (13), which means no matter how the load current changes, GBW is unchanged. It also can be illustrated in Fig. 6. The frequency of the output pole \( p_C \) may be higher than, lower than, or equal to the compensation zero \( z_C \) under different load conditions, but the frequency of GBW is constant. As long as the frequency of compensated zero \( f_{zc} \) is on the left of GBW, and the frequency of output zero \( f_{zo} \) is on the right of GBW, the phase margin of at least 45° will be get. In addition, regardless of the load resistor’s value, GBW is constant, so the controller system can be stable in any load conditions [17].

According to traditional design experience, the crossover frequency \( f_c \) is below 1/20 to 1/10 of switch frequency \( f_s \) and \( Z_o \) is placed out of GBW in any load conditions. Then \( f_{zc} \) is below 1/4 of crossover frequency \( f_c \). According to this compensation principle, the parameters of the compensate network \( A, f_0, R_C \) and \( C_C \) can be determined.

In the same way [27], the stability of buck method can be analyzed. The \( v(s)/i(s) \) of buck power stage is

\[ \frac{v(s)}{i(s)} = \frac{R}{1 + sRC}; \quad p_0 = \frac{1}{RC} \]

(14)

There is only one output pole and no zero. Thus, to achieve a high system stability is easier than in boost method. If the compensation network can ensure the stability of the boost method, it can also ensure the stability of the buck method.

Then come to the analysis of three-phase transition method. By the same analysis method [27], the \( v(s)/i(s) \) of the transition method is deduced as

\[ \frac{v(s)}{i(s)} = \frac{(1 - D_0 + D)(2 - D_0)R}{(3 - D_0 - D)} \left( 1 - \frac{s[(1 - D)L(1 - D_0 + D) + D^2(2 - D_0)R]}{(1 - D)L} \right) \]

(15)

There is also an output pole and a right-half-plan zero, shown as Eq. (16). Compared with the boost method and buck method, the poles and zeroes relationship is shown in Eq. (17): the output pole is between the buck and boost output poles, and the right-half-plan zero is on the right of the boost zero. So if the boost method is compensated, the transition method can be stable too

\[ p_0 = \frac{3 - D_0 - D}{(2 - D_0)RC}; \quad z_0 = \frac{(1 - D_0 + D^2(2 - D_0)R)}{(1 - D)L} \]

(16)

\[ \frac{1}{RC} < p_0 < \frac{2}{RC}; \quad \frac{z_0}{D^2} > \frac{1}{L} \]

(17)

From the analysis above, the traditional PI compensation can handle all the operation modes. The design of the compensation network should first satisfy the most likely unstable boost method, and then the stability of the other modes can be guaranteed.

3.2. Slope compensation

As we know, in valley or peak current programmed mode, when duty cycle of the first on switch is larger than 50%, slope compensation is needed. The analysis method is also suitable in the proposed three-phase transition method and will reach the similar conclusion.

Fig. 7 is the sketch chart of transition method starting up by buck discharge phase. If there is a small perturbation \( \Delta i(t) \) at \( t_0 \), the error current at \( nTs \) is

\[ \Delta i(nTs) = \left( \frac{-m_2}{m_1} \right)^n \Delta i(0) \]

(18)

\[ \frac{m_2}{m_1} = \frac{1 - D_0 + D}{1 - D} \]

(19)

\( D \) is the duty cycle of the first phase. The convergence condition for Eq. (18) is \( m_1 > m_2 \). Combined with Eq. (19), the convergence condition is \( D < 0.5D_0 \). So when the duty cycle is larger than 0.5D_0, slope compensation is needed. The compensated slope direction is
the dotted curve in Fig. 7. The direction is same for buck or boost method. In addition, the same results can be obtained in the transition method starting up by boost charge phase.

Based on the control method described in part 2, the slope direction is same for all four operation modes and the slope compensation circuit is uniform. Adding a negative ramp signal to the control signal is an ordinary method, and the minimum experience value of the \( m_g \) can be 0.5\( m_g \).

From the analysis of the loop compensation and slope compensation, the proposed control method cleverly covers all operation modes using one single control loop. Stability under all modes is achieved through applying one simple compensation method. In this way, circuit multi-utilization is realized to a great extent.

4. Integrated controller design

The circuit in the dotted square in Fig. 1 can be integrated onto a monolithic chip, which includes the basic function blocks such as band-gap reference, soft start, error amplifier, comparators and drivers. The structure of these basic blocks is so common that will not be detailedly introduced. However, the control logic is of much importance in such a multi-mode controller. Here finite state machine is introduced to implement the control. In addition, the VI (voltage to current) converter block is connecting the voltage loop and current loop. It is the most important block and will be described in detail together with current comparator in this section.

4.1. VI Converter and current comparator

According to the description of valley current programmed mode in buck and peak current programmed mode in boost in part 2, the combination of the two operation modes is mainly the VI converter and current comparator. The design aim of the VI converter and current comparator is to realize the function of Eqs. (1) and (2): plus EA_OUT signal to \( V_{SENSE} \) in buck method and minus it from \( V_{SENSE} \) in boost method. In the same time it is needed to deal with both negative and positive signal of \( V_{SENSE} \) without increasing complexity of the circuits. Moreover, the designed circuits should be suitable under each operation mode in all expected load conditions, since the average inductor current and current ripple are different between buck and boost even under the same load condition.

The VI converter implementation is shown in Fig. 8. Before the EA_OUT voltage being converted to current, it is added soft start and clamp functions. MP1–MP2 and MP3–MP5 are both smaller-pick pairs, one is two-inputs and another is three-inputs. When system starts up, these two pairs will select the SS (output of soft start circuit and is a linear increased voltage) signal to implement soft start function. When the EA_OUT is too high, the right pair will select the \( V_{max\_clamp} \) signal to realize over current protection. MN1–MN2 is a bigger-pick pair. In burst mode, the \( V_{min\_clamp} \) signal is selected when EA_OUT need to be clamped at a minimum value. Through selection, the output signal is \( I_{TH} \). The voltage to current function is realized through a common source structure with source degeneration by MN0 and \( R_{CV} \). The function is converting the \( I_{TH} \) voltage into current signal with a conversion ratio of

\[
G_m = \frac{g_m(MN0)}{1 + g_m(MN0)R_{VI}}
\]

Once \( I_c \) is generated, it is mirrored out in two directions, the push current and the pull current shown in the right part of the Fig. 8. This part is used to transfer different values of \( I_{TH} \) to buck or boost method. The four transfer gates are controlled by a BUCK or BOOST signal. This signal is generated in control logic to determine the converter working mode.

When BUCK is enabling, the transfer gates TC2 and TC3 are conductive and TC1 and TC4 are shut down. The current flowing from \( I^− \) and \( I^+ \) is as Eq. (21) shows:

\[
I^− = I_2 - I_c + I_4; \quad I^+ = I_1 + I_c + I_3
\]

Conversely, if BOOST is enabling, the conductive transfer gates are TC1 and TC4. The current flowing from \( I^− \) and \( I^+ \) is in Eq. (22):

\[
I^− = I_1 + I_c + I_4; \quad I^+ = I_2 - I_c + I_3
\]

The current \( I^− \) and \( I^+ \) generated in the VI converter will be the tail current in the input stage of the current comparator. The different value of \( I_{TH} \) will be reflected in the current comparator as the input offset voltage. Fig. 9 is the structure of the current comparator. The function of first stage is level shift, since the sensed voltage of \( SENSE^+ \) is too small to drive the second stage. The second stage, followed by an ordinary comparator, is to generate offset voltage between two inputs. Here choose bipolar transistor as input pair to achieve high comparator speed and low matching offset so that the total offset voltage is purely generated by circuit parameters.

The offset generator is quite important, and its principle is discussed below.

\( I_{Q1} \) and \( I_{Q2} \) are the currents flowing through the two input bipolar transistors:

\[
I_{Q1} = I^− - I_c; \quad I_{Q2} = I^+ + I_c
\]

Fig. 8. Functional diagram of VI converter.
\( I_s \) is the current flowing through \( R_s \), and can be expressed as
\[
I_s = \frac{V_f - V_e}{R_s} \tag{24}
\]

The voltages at points \( C \) and \( D \), \( E \) and \( F \) can be written as
\[
V_C = V_{DD} - R_3 I_{Q1} \tag{25}
\]
\[
V_D = V_{DD} - R_4 I_{Q2} \tag{26}
\]
\[
V_E = V_A - V_{be1} \tag{27}
\]

Assume that transistor \( Q_1 \) has the same size with \( Q_2 \), and further suppose that the comparator’s trip point is at where the voltage \( C \) is equal to \( D \). From Eq. (23)–(28), we can calculate the offset between point \( A \) and \( B \):
\[
V_B - V_A = R_5 \frac{R_3 I_1 - R_4 I_2^+}{R_3 + R_4} \tag{29}
\]

Since \( I_1 \) is equal to \( I_2 \); \( R_1 \) is equal to \( R_2 \), the offset between point \( A \) and \( B \) is also the offset between point \( SENSE^+ \) and \( SENSE^- \). Adding the condition that \( R_3 \) is equal to \( R_4 \), the final result is in Eq. (30). The offset between \( SENSE^+ \) and \( SENSE^- \) is exactly the value that should be shifted by \( ITH \) in buck or boost method:
\[
SENSE^+ - SENSE^- = \frac{R_5}{2} (I^- - I^+) \tag{30}
\]

Combining the conditions obtained from the analysis of VI converter, Eqs. (21) and (22), we can get the inductor current and \( ITH \) relation expressed by the circuit parameters. In buck method, the result is
\[
\left( I_L - \frac{1}{2} \Delta I \right) R_{SENSE} = \frac{R_5}{2} (I_4 - I_3 + I_2 - I_1 - 2I_C) \tag{31}
\]

In boost method, the expression is
\[
\left( I_L + \frac{1}{2} \Delta I \right) R_{SENSE} = \frac{R_5}{2} (I_4 - I_3 + I_1 - I_2 + 2I_C) \tag{32}
\]

According to the circuit analysis, Eqs. (31) and (32) have the same formation with Eqs. (1) and (2) from the system description. As far as designing reasonable values for the circuit parameters is concerned, the design target has been reached so as not to make the output of \( EA \) saturated in desired load range for each operation mode.
4.2. Finite state machine control principles

For multi-mode controllers, finite state machine is helpful to determine the circuit configurations of the power stage. Fig. 10 is the state transition graph for the forced continuous current mode operation. The transition rules of this state machine are based on the system modeling mentioned in part 2. In a word, they judge the duty cycle to determine and change the operation modes.

The finite state machine has five states defined as shut down state, buck state, boost state and two transition states. Every state is assigned a unique state code. \( C_0, C_1 \) and \( C_2 \) represent the percentage of the duty cycle, which can be obtained from the comparison between duty cycle and timers. The state output is not only related to input conditions but also related to the previous state. It is a Mealy machine.

Since there is soft start function (which is implemented by RUN/SS block) to linearly increase the output voltage to prevent overshoot during controller starting up, the state goes to buck method when starting up no matter what the input voltage is. If the duty cycle remains at position \( C_0 \), the converter works in buck method. If \( V_{IN} \) decreases or \( V_{OUT} \) increases, the duty cycle will turn into position \( C_1 \) and the converter will work in three-phase transition method starting with buck discharge phase. When the duty cycle further decreases, the state goes into boost method for at least one cycle. In this cycle, the controller judges the duty cycle again and determines whether the next cycle stays in boost method or transitions to the three-phase transition method starting with boost charge phase. Transition from boost method back to buck method takes place in the opposite process.

Once the operation mode is determined, other control logic can be easily generated through combinational logic of the state variables, such as \( BUCK \) or \( BOOST \) signal for VI converter, driver signals, shut down signal and so on.

5. Converter design and experimental results

The prototype IC of the proposed controller is fabricated in a 1.5-\( \mu \)m double-metal single-poly BCD process with an area of 8.75 mm\(^2\). The die microphotograph of the chip is shown in Fig. 11. Except 8 application defined pins, all the rest is added for testing or as power supply pins. A 2.7–4.2 V/3.3 V 4-switch buck–boost converter suitable for Li-ion battery power supplies is constructed using this IC. The topology of the converter is also built as shown in Fig. 1. The output load range is set to 0–500 mA to fit normal portable apparatuses. Its output voltage is adjusted via a feedback resistor divide. The four switches are off-chip CMOS switches: TG1 and TG2 are P-channel MOSFETs; BG1 and BG2 are N-channel MOSFETs. The key parameters are listed in Table 1.

5.1. Multi-mode operation

Experimental results of the converter with the proposed multi-mode control in forced CCM for \( V_{IN} \) below, above or equal to \( V_{OUT} \) at the load of 300 mA are shown in Figs. 12–15, respectively. In the test, the parasitic parameters such as equivalent series resistor (ESR) and equivalent series inductor (ESL) are inevitable, so the performance like ripple voltage is not as good as ideal situation.

Fig. 12 is under 4.2 V input condition. The converter works in the proposed valley current programmed buck method and outputs 3.3 V steadily with about 5.6 mV ripple. In buck converters, the output ripple is independent of variables, such as load current. As shown in Eq. (33), if the parameters of the converter are determined, the ripple is constant. Furthermore, there are only two switches operating every cycle, and the switch loss can be reduced significantly

\[
\Delta U_c = \frac{\Delta I}{8fC_{load}} \tag{33}
\]

If \( V_{IN} \) decreases and gets close to \( V_{OUT} \), the converter goes into the three-phase transition method starting with buck discharge phase. Fig. 13 is the testing result of 3.4 V input voltage. The output voltage is still stable and with a ripple of 6.2 mV. The approximate expression of ripple voltage under this mode is in Eq. (34). Though it is dependent on load current, but the factor of \((D_0-D)\) is small under this transition method, so the ripple voltage

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_1 )</td>
<td>15 ( \mu )H</td>
</tr>
<tr>
<td>( C_{OUT} )</td>
<td>30 ( \mu )F</td>
</tr>
<tr>
<td>( R_{sen} )</td>
<td>100 m( \Omega )</td>
</tr>
<tr>
<td>( R_1 )</td>
<td>200 k( \Omega )</td>
</tr>
<tr>
<td>( f_{clock} )</td>
<td>400 kHz</td>
</tr>
<tr>
<td>( R_{DS1} )</td>
<td>70 m( \Omega )</td>
</tr>
<tr>
<td>( R_{DS2} )</td>
<td>40 m( \Omega )</td>
</tr>
<tr>
<td>( R_{f1} )</td>
<td>100 k( \Omega )</td>
</tr>
<tr>
<td>( R_{f2} )</td>
<td>200 k( \Omega )</td>
</tr>
</tbody>
</table>

Fig. 11. Chip microphotograph.

Fig. 12. Test waveform of buck mode.
will not be large. It is also shown that the inductor current has three operation phases and in this mode BG2 and BG1 are both switching

\[
\Delta U_C = \frac{I_{load}(D_0 - D)}{R_{Load}}
\]

If VIN further decreases to below VOUT, the converter works in the three-phase transition method starting with boost charge phase. As Fig. 14 shows, it is the testing result at 3.2 V input voltage and 3.3 V output voltage with 8.4 mV ripple. The ripple voltage expression is Eq. (35), and the duty cycle is also small under this transition method, so is ripple voltage. Similar to another transition method, the inductor current also has three operation phases and both BG2 and BG1 are switching.

\[
\Delta U_C = \frac{I_{load}D}{R_{Load}}
\]

When VIN decreases to far from VOUT, 2.7 V typically, the converter will work in boost method, and Fig. 15 is its testing result. In boost method, the output voltage is still stable but the ripple voltage is dependent on load current and duty cycle as
All the testing results show that the function of multi-mode operation has been achieved. Then converter can switch from buck to boost and back to buck automatically and the seamless transition has been realized. It is also proved that the proposed transition method has smaller ripple voltage than purely boost method or traditional buck-boost method.

Fig. 16 shows the testing results of high efficiency burst mode operation under light-load condition. In the design, when the average inductor current falls below 100 mA, the converter will turn into burst mode automatically. In burst mode, the minimum valley current of buck method and the maximum peak current of boost method are clamped. In buck converter, the average inductor current is equal to load current. So the buck method will turn into burst operation when load current falls below 100 mA. But in boost converter, the average inductor current is about \( \frac{V_{OUT}}{V_{IN}} \) times of load current. So the mode transition point of load current will be a little lower than that of the buck method, which is about 75 mA with input voltage of 2.7 V. The test is carried out under 30 mA load current. It is obvious that the converter works in several cycles and shuts down several cycles, thus effectively reduces the switch loss. The output ripple voltage is mainly decided by the hysteresis window of \( BURST \) comparator, which is about 80 mV. Burst mode has higher ripple voltage than forced CCM, but more efficient than CCM. So which operation mode should be used is dependent on the applications.

Fig. 17 shows the line regulation of the converter, with only 4 mV variation in the input voltage range of 2.7–4.2 V, during which the operation mode is changing. Fig. 18 is the load regulation of the converter. The output voltage has variation of 0.27% max in buck method and 0.45% in boost method during the load range of 0–500 mA.

5.2. Stability and transient response performance

According to the stability analysis in part 3, the PI compensation network is introduced. The values of \( R_C \) and \( C_C \) in Fig. 5 are chosen to be 20 k\( \Omega \) and 1 nF. Fig. 19 is the testing results of the open loop stability under 300 mA load condition of buck method and boost method. The crossover frequency and the phase margin are shown in the figures. Since the transfer function of power stage is different between buck and boost converters, the stability characteristics will have a little difference under the same compensation network. But according to the compensation
theory, if the boost method is stable, the buck method and transition method will also be stable.

Based on this compensation network, the load step performance is shown in Fig. 20. In the test, the load current is switched between 30 and 300 mA with a slew rate of 80 mA/μs. Under 45–55° phase margin, the transient response will have a little over modulation but less settling time. The load step transient response performances are listed in Table 2.

5.3. Converter efficiency

The conversion efficiency curve of the proposed design is shown in Fig. 21, together with the ones of the forced continuous current mode and high efficiency burst mode design. It can be observed that the forced CCM design with constant frequency control over the entire load range suffers from efficiency degradation with load decreasing. Under light-load condition, when the forced CCM makes the inductor current reverse, part of the power flows into the ground in buck method and into input power.

![Fig. 20. Test waveform of load step: (a) load step in buck mode and (b) load step in boost mode.](image)

![Table 2](image)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
<th>Buck mode</th>
<th>Boost mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Droop voltage at 30 mA – 300 mA step</td>
<td>210 nV</td>
<td>220 nV</td>
<td></td>
</tr>
<tr>
<td>Recovery time at 30 mA – 300 mA step</td>
<td>100 μs</td>
<td>70 μs</td>
<td></td>
</tr>
<tr>
<td>Overshoot voltage at 300 mA – 30 mA step</td>
<td>270 mV</td>
<td>250 mV</td>
<td></td>
</tr>
<tr>
<td>Recovery time at 300 mA – 30 mA step</td>
<td>88 μS</td>
<td>64 μS</td>
<td></td>
</tr>
</tbody>
</table>

![Fig. 21. Test result of efficiency: (a) buck mode efficiency and (b) boost mode efficiency.](image)

![Table 3](image)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{in})</td>
<td>205 V–4.2 V</td>
</tr>
<tr>
<td>(V_{out})</td>
<td>3.3 V</td>
</tr>
<tr>
<td>(I_{load})</td>
<td>0–500 mA</td>
</tr>
<tr>
<td>Line regulation</td>
<td>Max: 4 mV</td>
</tr>
<tr>
<td>Load regulation</td>
<td>Max: 9 mV (buck)</td>
</tr>
<tr>
<td>Efficiency ((I_{load}=5–500\ mA))</td>
<td>&gt; 90% in heavy load</td>
</tr>
<tr>
<td></td>
<td>&gt; 80% in light load under burst mode</td>
</tr>
</tbody>
</table>
supply in boost method. So in boost method, the efficiency will not decrease so fast as buck method does. The comparison shows that the burst mode achieves a high efficiency of over 80% from full load down to no-load, with a peak of 93% in buck method and 94% in boost method. It also can be expected that by optimizing the on-resistance of power switches, ESR of inductor and capacitor, and sensing resistor, it is possible to further reduce the conductive power loss over the entire load range and achieve higher conversion efficiency [26].

5.4. Performance summary

Table 3 summarizes the main performance of the converter design. The converter features excellent line regulation and load regulation. The transient response is satisfactory, and high efficiency is also achieved.

5.5. Performance comparison

Finally, Table 4 compares this work with prior arts. The comparison mainly focuses on the performance of output ripple, transient response and efficiency. Most of the control method applied in the 4-switch buck–boost topology is voltage mode since it is much simpler than current mode. This paper applied current mode to achieve a higher transient response. The three-phase transition method helps to realize lower output ripple voltage, especially in the transition mode; the ripple voltage is much lower than other arts. Furthermore, the introduction of burst mode evidently increases the light load efficiency for portable applications.

6. Conclusion

This paper proposed a novel multi-mode step down/step up controller IC and applied it to a 4-switch cascade buck–boost converter. By limiting the duty cycles of buck and boost method, respectively, automatic mode transition can be realized. The three-phase operation mode was introduced to implement seamless transition and lower output ripple. The mode transition is controlled by a finite state machine. In addition, high efficiency burst mode is applied to further reduce the switch loss in light-load and standby occasions.

The loop and slope compensation analysis guarantee the regular and stable work of the system. The control method design and silicon implementation realize the multi-utilization perfectly. The controller IC was designed and fabricated in 1.5-μm BCD technology. The experimental results verified the merits of the proposed design. The low ripple and excellent line regulation with an error of ± 0.06% max is achieved during multi-mode operation of the buck–boost converter. Moreover, high efficiency of over 80% has been reached from full load down to no-load.

Acknowledgments

The project gains support from the National Semiconductor Corp. (NSC). The authors would like to thank Mr. David Pace and Mr. Guy Cheung, the senior engineers of NSC, for their helpful discussions and instructions.

References


